Amendments to the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

Claim 1 (previously presented) A cache controller for use with a processor, comprising:

a plurality of mappers for receiving instructions of an instruction set, each mapper for mapping an instruction of said instruction set to a predetermined instruction width format (PIWF) configuration, wherein said plurality of mappers include

at least one first mapper for receiving instructions from a fill buffer, and

at least one second mapper for receiving instructions from an instruction cache; and

a multiplexor for receiving said PIWF configurations from said plurality of mappers and selecting, in response to a selector signal, a desired one of said PIWF configurations for decoding and execution by the processor.

Claim 2 (original) The cache controller of claim 1, further comprising:

a tag comparator for generating said selector signal.

Claim 3 (previously presented) The cache controller of claim 2, wherein said tag comparator comprises:

means for comparing, for each instruction provided to one of said plurality of mappers, a tag associated with an instruction of said instruction set to a desired tag and

generating said selector signal to cause said multiplexor to select said desired one of said PIWF configurations.

Claim 4 (canceled)

Claim 5 (previously presented) In a cache controller for use with a processor, a method for mapping an instruction set to a predetermined instruction width format (PIWF) configuration, comprising:

(a) reading instructions of said instruction set from an instruction cache and a fill buffer into a plurality of mappers, wherein at least one of said instructions is read from said instruction cache and at least one of said instructions is read from said fill buffer, each instruction of said instruction set being read into a corresponding one of said plurality of mappers in preparation for mapping;

(b) mapping each instruction of said instruction set to a corresponding PIWF configuration; and

(c) selecting a desired one of said PIWF configurations for decoding and execution by the processor.

Claim 6 (previously presented) The method of claim 5, further comprising:

(d) comparing, for each instruction provided to one of said plurality of mappers, a tag associated with an instruction of said instruction set to a desired tag, wherein said desired one of said PIWF configurations is selected based on said comparison.

Claim 7 (canceled)

Claim 8 (previously presented) A processor comprising:

an execution unit;

a decoder;

a cache for storing instructions; and

a cache controller for retrieving said instructions from said cache and providing said instructions to said decoder, said cache controller comprising:

a plurality of mappers for mapping a plurality of instructions of an instruction set to predetermined instruction width format (PIWF) configurations, said plurality of mappers including at least one first mapper for receiving instructions from a fill buffer, and at least one second mapper for receiving instructions from said instruction cache,

a multiplexor for selecting, in response to a selector signal, one of said PIWF configurations for decoding by said decoder and execution by said execution unit, and

means for comparing, for each instruction provided to said multiplexor, a tag associated with an instruction of said instruction set to a desired tag and generating said selector signal to cause said multiplexor to select said desired one of said PIWF configurations,

whereby said processor performs instruction mapping substantially in parallel with tag comparison to improve processor performance.

Claim 9 (canceled)

Claim 10 (currently amended) A tangible computer readable storage medium comprising a microprocessor core embodied in software, said microprocessor core including a cache controller comprising:

a plurality of mappers for receiving instructions of an instruction set, each mapper for mapping an instruction of said instruction set to a predetermined instruction width format (PIWF) configuration, wherein said plurality of mappers include

at least one first mapper for receiving instructions from a fill buffer, and

at least one second mapper for receiving instructions from an instruction cache; and

a multiplexor for receiving said PIWF configurations from said plurality of mappers and selecting, in response to a selector signal, a desired one of said PIWF configurations for decoding and execution by said microprocessor core.

Claim 11 (currently amended) The tangible computer readable storage medium of claim 10, wherein said cache controller further comprises:

a tag comparator, configured to compare, for each instruction provided to one of said plurality of mappers, a tag associated with an instruction of said instruction set to a desired tag and to generate said selector signal to cause said multiplexor to select said desired one of said PIWF configurations.

Claim 12 (currently amended) The tangible computer readable storage medium of claim 10, wherein said microprocessor core is embodied in hardware description language software.

Claim 13 (currently amended) The tangible computer readable storage medium of claim 12, wherein said microprocessor core is embodied in Verilog hardware description language software.

Claim 14 (currently amended) The tangible computer readable storage medium of claim 12, wherein said microprocessor core is embodied in VHDL hardware description language software.

Claims 15-20 (canceled)

Claim 21 (new) A method for decoding instructions in a processor, comprising:

(a) mapping each of a plurality of instructions to a predetermined instruction width format (PIWF) configuration;

(b) comparing, in parallel with (a), a tag for each of said plurality of instructions to an address;

(c) selecting, based on the comparison in (b), one of the PIWF configurations of (a) to be decoded; and

(d) decoding the PIWF configuration selected in (c).

Claim 22 (new) The method of claim 21, wherein (a) comprises mapping a plurality of 16-bit instructions to a plurality of PIWF configurations.

Claim 23 (new) The method of claim 21, wherein (a) comprises mapping a plurality of 32-bit instructions to a plurality of PIWF configurations.

Claim 24 (new) The method of claim 21, wherein (a) comprises mapping an instruction from a fill buffer to a PIWF configuration.

Claim 25 (new) The method of claim 21, wherein (a) comprises mapping a 16-bit instruction to a PIWF configuration that has more than 32-bits.

Claim 26 (new) The method of claim 21, wherein (a) comprises mapping a 32-bit instruction to a PIWF configuration that has more than 32-bits.

Claim 27 (new) The method of claim 21, wherein (a) comprises performing a first partial mapping in parallel with (b), and performing a second partial mapping after (c).

Claim 28 (new) A cache controller for use with a processor, comprising:

means for mapping each of a plurality of instructions to a predetermined instruction width format (PIWF) configuration; and

a multiplexor for receiving said PIWF configurations from said means for mapping and for selecting, in response to a selector signal, a desired one of said PIWF configurations for decoding and execution by the processor.

Claim 29 (new) The method of claim 28, wherein said means for mapping maps an instruction from a fill buffer to a PIWF configuration.